

REMARKS

The applicants appreciate the careful examination the Examiner has given to this application and believe the claims as amended will satisfy the Examiner's
5 concerns. In the examination report, the Examiner has stated that claims 9-14, 26-36 and 41-42 are allowable subject matter.

Accordingly, claims 9, 26 and 41 have been re-written in independent form including all limitations of the base claim and intermediate claims as suggested
10 by the Examiner. Thus, claims 9-14, 26-36 and 41-42 shall be now allowable.

The Examiner has also requested the corrected drawings to show every feature of the invention specified in the claims.

In response to this request, the inventors have double checked the drawings and confirmed that all features of the amended claims are shown in the
15 drawings, e.g. all features of claim 9 are collectively shown in Figures 4A to 9, though different features of claim 9 may be shown in different drawings, e.g. forming k=3 stages is illustrated in Figures 3C and 8A, and grouping within a stage into blocks, sub-blocks and sub-sub-blocks is shown in Figures 4A and 9.

If the Examiner disagrees with the above comments regarding the
20 drawings, then the Applicant respectfully asks if the Examiner could be more specific what features of which claim(s) the Examiner considers missing from the drawings, and the Applicants will amend the drawings accordingly.

An early allowance is respectfully requested.

25 The Commissioner is hereby authorized to deduct any prescribed fees for these amendments, if required, from our Company's Deposit Account No. 501832.

Yours truly,
Dongxing Jin

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By: _____

Victoria Donnelly, Ph.D.

WE CLAIM:

1. (canceled) A method of performing a k-stage FFT (fast Fourier transform) computation of N data points wherein k and N are integers, the method comprising:
 - performing a plurality of operations upon the N data points, each one of the plurality of operations comprising:
 - _____ performing an import of a respective plurality of sets of data points of the N data points from an external memory into an internal memory;
 - _____ performing a FFT computation of the k-stage FFT computation upon each one of the sets of data points in the internal memory; and
 - _____ performing an export of the respective plurality of sets of data points of the N data points from the internal memory into the external memory to update the respective sets of data points of the N data points in the external memory.
2. (canceled) A method of performing a k-stage FFT computation of N data points wherein k and N are integers, the method comprising:
 - _____ for each one of a plurality of stage groupings of at least one stage of k stages of the k-stage FFT computation wherein the plurality of stage groupings of at least one stage collectively comprise the k stages, performing a respective plurality of operations on the N data points, each one of the respective plurality of operations comprising:
 - _____ performing an import of a respective plurality of sets of data points of the N data points from an external memory into an internal memory;
 - _____ performing a FFT computation upon each one of the respective plurality of sets of data points of the N data points in the internal memory; and

~~performing an export of the respective plurality of sets of data points of the N data points from the internal memory into the external memory to update the respective plurality of sets of data points of the N data points in the external memory.~~

3. (canceled) ~~A method of performing a k-stage FFT computation according to claim 2 comprising performing an import of a next respective plurality of sets of data points of the N data points for a next one of the respective plurality of operations while the performing a FFT computation upon each one of the respective plurality of sets of data points of the N data points in the internal memory.~~
4. (canceled) ~~A method of performing a k-stage FFT computation according to claim 2 comprising performing an export of a previous respective plurality of sets of data points of the N data points for a previous one of the respective plurality of operations while the performing a FFT computation upon each one of the respective plurality of sets of data points of the N data points in the internal memory.~~
5. (canceled) ~~A method of performing a k-stage FFT computation according to claim 2 wherein the FFT computation is performed using decimation in frequency (DIF).~~
6. (canceled) ~~A method of performing a k-stage FFT computation according to claim 2 wherein the FFT computation is performed using decimation in time (DIT).~~
7. (canceled) ~~A method of performing a k-stage FFT computation according to claim 2 wherein N substantially satisfies $N = 2^k$.~~
8. (canceled) ~~A method of performing a k-stage FFT computation according to claim 7 wherein the stage groupings of at least one stage comprise Q stage groupings each comprising S stages, said Q and said S being integers with $Q \geq 1$, $S \geq 1$ and $k \geq QS$.~~
9. (currently amended) A method of performing a k-stage FFT computation according to claim 8 of N data points wherein k and N are integers, the method comprising: for each one of a plurality of stage groupings of at least one stage of k stages of the k-stage FFT computation wherein the plurality of stage groupings of at least one stage collectively comprise the k stages, performing a respective plurality of operations

on the N data points, each one of the respective plurality of operations comprising:
performing an import of a respective plurality of sets of data points of the N data points
from an external memory into an internal memory; performing a FFT computation upon
each one of the respective plurality of sets of data points of the N data points in the
internal memory; and performing an export of the respective plurality of sets of data
points of the N data points from the internal memory into the external memory to update
the respective plurality of sets of data points of the N data points in the external memory;
wherein the stage groupings of at least one stage comprise Q stage groupings each
comprising S stages, said Q and said S being integers with $Q \geq 1$, $S \geq 1$ and $k \geq QS$; and
wherein N substantially satisfies $N = 2^k$, comprising:

grouping, within a stage grouping, I, of the Q stage groupings wherein I is an integer satisfying $0 \leq I \leq Q-1$, the N data points into 2^{IS} blocks of data of $N/2^{IS}$ respective data points;

grouping, within each one of the 2^{IS} blocks of data, the $N/2^{IS}$ respective data points into 2^S sub-blocks of data of $N/2^{IS+S}$ respective data points;

grouping, within each one of the 2^S sub-blocks of data, the $N/2^{IS+S}$ respective data points into M_1 sub-sub-blocks of data of $N/(2^{IS+S} M_1)$ respective data points wherein M_1 is an integer;

taking, within each one of the 2^{IS} blocks of data, a respective sub-sub-block of data of the M_1 sub-sub-blocks of data from each one of the 2^S sub-blocks of data to form a set of 2^S sub-sub-blocks of data of $N/(2^{IS} M_1)$ data points a total of M_1 times to produce M_1 sets of 2^S sub-sub-blocks of data of $N/(2^{IS} M_1)$ data points; and

taking, within each one of the M_1 sets of 2^S sub-sub-blocks of data, a respective data point from each one of the 2^S sub-blocks of data to form a set of 2^S data points a total of $N/(2^{IS+S} M_1)$ times to produce $N/(2^{IS+S} M_1)$ sets of 2^S data points.

10. (original) A method of performing a k-stage FFT computation according to claim 9 wherein, for the stage grouping, I, of the Q stage groupings of the plurality of stage groupings, the performing a respective plurality of operations on the N data points

comprises performing M_1 of the plurality of operations for each one of the 2^{IS} blocks of data within the stage grouping, I, each one of the M_1 of the plurality operations comprising:

performing an import of respective $N/(2^{IS+S}M_1)$ sets of 2^S data points from the external memory into the internal memory;

performing an S-stage FFT computation of the k-stage FFT computation upon each set of 2^S data points of the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points in the internal memory; and

performing an export of the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points from the internal memory into the external memory to update the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points in the external memory.

11. (original) A method of performing a k-stage FFT computation according to claim 10 wherein M_1 substantially satisfies $M_1 = N/(2^{IS}M_1)$ wherein M_1 corresponds to the number of data points the internal memory can hold.

12. (original) A method of performing a k-stage FFT computation according to claim 10 wherein M_1 substantially satisfies $M_1 = N/(2^{IS-1}M_1)$ wherein M_1 corresponds to the number of data points a buffer in the internal memory can hold.

13. (original) A method of performing a k-stage FFT computation according to claim 10 wherein the performing an S-stage FFT computation of the k-stage FFT computation upon each set of 2^S data points of the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points results in $N/(2^{IS+S}M_1)$ S-stage FFT computations, the $N/(2^{IS+S}M_1)$ S-stage FFT computations comprising performing one stage of S stages for each one of the $N/(2^{IS+S}M_1)$ S-stage FFT computations and iterating through the S stages.

14. (original) A method of performing a k-stage FFT computation according to claim 10 wherein the performing an S-stage FFT computation of the k-stage FFT computation upon each set of 2^S data points of the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points results in $N/(2^{IS+S}M_1)$ S-stage FFT computations, the $N/(2^{IS+S}M_1)$ S-stage FFT computations

comprising performing computations for S stages of an S-stage FFT computation of one of the $N/(2^{IS+S} M_1)$ S-stage FFT computations before another S-stage FFT computation is performed on another of one of the $N/(2^{IS+S} M_1)$ S-stage FFT computations.

15. (canceled) A method of performing a k-stage FFT computation according to claim 8 wherein the stage groupings of at least one stage comprise a stage grouping comprising D stages wherein D is an integer and $k=QS+D$.

16. (canceled) A method of performing a k-stage FFT computation according to claim 15 wherein the performing an import comprises importing the plurality of sets of data points into a buffer in the internal memory, the buffer having a capacity to hold M_1 data points and D being an integer substantially satisfying $D \leq \log_2(M_1)$.

17. (canceled) A method of performing a k-stage FFT computation according to claim 15 wherein the performing an import comprises importing the plurality of sets of data points into one of two buffers of a double buffer in the internal memory, each one of the two buffers having a capacity to hold $M_1/2$ data points and D being an integer substantially satisfying $D \leq \log_2(M_1/2)$.

18. (canceled) A method of performing a k-stage FFT computation according to claim 15 comprising, for each one of a plurality of sub-stage groupings of at least one stage of the stage grouping of D stages wherein the plurality of sub-stage groupings of at least one stage collectively comprise the D stages, performing a set of sub-stage FFT computations wherein for each one of the sub-stage FFT computations respective data points and respective twiddle factors are loaded into a high-speed cache.

19. (canceled) A processing platform implementing the method of claim 2.

20. (canceled) A processor comprising:

an internal memory adapted to store data;

a DMA (direct memory access) unit adapted to import data into the internal memory and to export data from the internal memory; and

_____ a central processor unit (CPU) adapted to perform, for each one of a plurality of stage groupings of at least one stage of k stages of the k-stage FFT computation wherein the plurality of stage groupings of at least one stage collectively comprise the k stages, a respective plurality of operations on the N data points, for each one of the respective plurality of operations the CPU is adapted to:

_____ provide instructions to the DMA unit for performing an import of a respective plurality of sets of data points, of N data points, into the internal memory;

_____ perform a FFT computation upon each one of the respective plurality of sets of data points, of the N data points, in the internal memory; and

_____ provide instructions to the DMA unit for performing an export of the respective plurality of sets of data points, of the N data points, from the internal memory to update the respective plurality of sets of data points of the N data points.

21. (canceled) A processor according to claim 20 further comprising an external memory adapted to store the N data points.

22. (canceled) A processor according to claim 21 comprising at least one bus wherein the DMA unit is further adapted to import the respective plurality of sets of data points, of the N data points, from the external memory and to export the respective plurality of sets of data points, of the N data points, into the external memory through the at least one bus.

23. (canceled) A processor according to claim 20 wherein the internal memory comprises:

_____ a double buffer comprising two buffers each adapted to stored data points;

_____ two buses each adapted to provide a channel for importing the data points into a respective one of the two buffers and for exporting the data points from the respective one of the two buffers; and

_____ the CPU being further adapted to provide instructions to the DMA unit for importing a respective plurality of sets of data points, of the N data points, into one of the

~~two buffers while the CPU performs FFT computations upon another respective plurality of sets of data points, of the N data points, stored in another one of the two buffers.~~

24. (canceled) A processor according to claim 20 wherein the internal memory comprises:

~~a double buffer comprising two buffers each adapted to store data points;~~

~~two buses each adapted to provide a channel for importing the data points into a respective one of the two buffers and for exporting the data points from the respective one of the two buffers; and~~

~~the CPU being further adapted to provide instructions to the DMA unit for exporting respective sets of data points from one of the two buffers while the CPU performs FFT computations upon other respective sets of data points stored in another one of the two buffers.~~

25. (canceled) A processor according to claim 20 wherein N substantially satisfies $N = 2^k$ with k being an integer and wherein the stage groupings of at least one stage comprise Q stage groupings each comprising S stages, said Q and said S being integers with $Q \geq 1$, $S \geq 1$ and $k \geq QS$.

26. (currently amended) A processor according to claim 20 comprising an internal memory adapted to store data; a DMA (direct memory access) unit adapted to import data into the internal memory and to export data from the internal memory; and a central processor unit (CPU) adapted to perform, for each one of a plurality of stage groupings of at least one stage of k stages of the k -stage FFT computation wherein the plurality of stage groupings of at least one stage collectively comprise the k stages, a respective plurality of operations on the N data points, for each one of the respective plurality of operations the CPU is adapted to: provide instructions to the DMA unit for performing an import of a respective plurality of sets of data points, of N data points, into the internal memory; perform a FFT computation upon each one of the respective plurality of sets of data points, of the N data points, in the internal memory; and provide instructions to the DMA unit for performing an export of the respective plurality of sets of data points, of

the N data points, from the internal memory to update the respective plurality of sets of data points of the N data points, wherein the CPU is adapted to:

group, within a stage grouping, I, of the Q stage groupings wherein I is an integer satisfying $0 \leq I \leq Q-1$, the N data points into 2^{IS} blocks of data of $N/2^{IS}$ respective data points;

group, within each one of the 2^{IS} blocks of data, the $N/2^{IS}$ respective data points into 2^S sub-blocks of data of $N/2^{IS+S}$ respective data points;

group, within each one of the 2^S sub-blocks of data, the $N/2^{IS+S}$ respective data points into M_1 sub-sub-blocks of data of $N/(2^{IS+S} M_1)$ respective data points wherein M_1 is an integer;

take, within each one of the 2^{IS} blocks of data, a respective sub-sub-block of data of the M_1 sub-sub-blocks of data from each one of the 2^S sub-blocks of data to form a set of 2^S sub-sub-blocks of data of $N/(2^{IS} M_1)$ data points a total of M_1 times to produce M_1 sets of 2^S sub-sub-blocks of data of $N/(2^{IS} M_1)$ data points; and

take, within each one of the M_1 sets of 2^S sub-sub-blocks of data, a respective data point from each one of the 2^S sub-blocks of data to form a set of 2^S data points a total of $N/(2^{IS+S} M_1)$ times to produce $N/(2^{IS+S} M_1)$ sets of 2^S data points.

27. (original) A processor according to claim 26 wherein, for the stage grouping, I, of the Q stage groupings of the plurality of stage groupings, the CPU is adapted to perform M_1 of the plurality operations for each one of the 2^{IS} blocks of data within the stage grouping, I, and for each one of the M_1 of the plurality operations the CPU is adapted to:

provide instructions to the DMA unit for performing an import of respective $N/(2^{IS+S} M_1)$ sets of 2^S data points into the internal memory;

performing an S-stage FFT computation of the k-stage FFT computation upon each set of 2^S data points of the respective $N/(2^{IS+S} M_1)$ sets of 2^S data points in the internal memory; and

provide instructions to the DMA unit for performing an export of the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points from the internal memory to update the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points.

28. (original) A processor according to claim 27 wherein the internal memory comprises a buffer adapted to store the plurality of sets of data points, wherein the buffer has a capacity to hold M_1 data points and M_1 substantially satisfies $M_1 = N/(2^{IS}M_1)$ wherein M_1 is an integer.

29. (original) A processor according to claim 27 wherein the internal memory comprises a double buffer adapted to store the plurality of sets of data points, wherein the double buffer comprises two buffers each capable of storing $M_1/2$ data points and wherein said M_1 substantially satisfies $M_1 = N/(2^{IS-1}M_1)$, M_1 being an integer.

30. (original) A processor according to claim 29 wherein while the CPU performs the S-stage FFT computation of the k-stage FFT computation upon each set of 2^S data points of the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points, the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points being stored in one of the two buffers, the CPU is adapted to provide instructions to the DMA unit to import, into another one of the two buffers, respective $N/(2^{IS+S}M_1)$ sets of 2^S data points of a next one of the each one of the M_1 of the plurality operations.

31. (original) A processor according to claim 29 wherein while the CPU performs the S-stage FFT computation of the k-stage FFT computation upon each set of 2^S data points of the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points, the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points being stored in one of the two buffers, the CPU is adapted to provide instructions to the DMA unit to export, from another one of the two buffers, respective $N/(2^{IS+S}M_1)$ sets of 2^S data points from previous one of the each one of the M_1 of the plurality operations.

32. (original) A processor according to claim 27 wherein the performing an S-stage FFT computation of the k-stage FFT computation upon each set of 2^S data points of the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points results in $N/(2^{IS+S}M_1)$ S-stage FFT computations, the CPU being further adapted to evaluate the $N/(2^{IS+S}M_1)$ S-stage FFT

computations at one stage of S stages for each one of the $N/(2^{IS+S} M_1)$ S-stage FFT computations and iterate through the S stages.

33. (original) A processor according to claim 27 wherein the internal memory comprises a high-speed cache.

34. (original) A processor according to claim 33 wherein the performing an S-stage FFT computation of the k-stage FFT computation upon each set of 2^S data points of the respective $N/(2^{IS+S} M_1)$ sets of 2^S data points results in $N/(2^{IS+S} M_1)$ S-stage FFT computations, the CPU being further adapted to perform computations for S stages of an S-stage FFT computation of one of the $N/(2^{IS+S} M_1)$ S-stage FFT computations before performing another S-stage FFT computation of another one of the $N/(2^{IS+S} M_1)$ S-stage FFT computations.

35. (original) A processor according to claim 28 wherein the stage groupings of at least one stage comprise a stage grouping of D stage wherein D is an integer, said k substantially satisfying $k=QS+D$ and said D substantially satisfying $D \leq \log_2(M_1)$.

36. (original) A processor according to claim 29 wherein the stage groupings of at least one stage comprise a stage grouping of D stage wherein D is an integer, said k substantially satisfying $k=QS+D$ and said D substantially satisfying $D \leq \log_2(M_1/2)$.

37. (canceled) ~~A processor according to claim 20 wherein the CPU is adapted to produce the k-stage FFT computation in real time.~~

38. (canceled) ~~A processor according to claim 20 wherein the internal memory comprises a buffer adapted to store twiddle factors used in the FFT computations.~~

39. (canceled) ~~An article of manufacture comprising:~~

~~a computer usable medium having computer readable program code means embodied therein for performing a k-stage FFT computation of N data points wherein k and N are integers, the computer readable code means in said article of manufacture comprising:~~

~~computer readable code FFT means for performing, for each one of a plurality of stage groupings of at least one stage of k stages of the k-stage FFT computation wherein the plurality of stage groupings of at least one stage collectively comprise the k stages, a respective plurality of operations on the N data points, for each one of the respective plurality of operations the computer readable code FFT means comprising:~~

~~computer readable code means for providing instructions for performing an import of a respective plurality of sets of data points of the N data points from an external memory into an internal memory;~~

~~computer readable code means for performing a FFT computation upon each one of the respective plurality of sets of data points of the N data points in the internal memory, and~~

~~computer readable code means for providing instructions for performing an export of the respective plurality of sets of data points of the N data points from the internal memory into the external memory to update the respective plurality of sets of data points of the N data points in the external memory.~~

40. (canceled) ~~An article of manufacture according to claim 39 wherein the stage groupings of at least one stage comprise a stage grouping of D stage and Q stage groupings of S stages wherein D, Q and S are integers and wherein said k substantially satisfies $k=QS+D$ and $k = \log_2(N)$.~~

41. (currently amended) ~~An article of manufacture according to claim 40 comprising a computer usable medium having computer readable program code means embodied therein for performing a k-stage FFT computation of N data points wherein k and N are integers, the computer readable code means in said article of manufacture comprising computer readable code FFT means for performing, for each one of a plurality of stage groupings of at least one stage of k stages of the k-stage FFT computation wherein the plurality of stage groupings of at least one stage collectively comprise the k stages, a respective plurality of operations on the N data points, for each~~

one of the respective plurality of operations the computer readable code FFT means comprising computer readable code means for providing instructions for performing an import of a respective plurality of sets of data points of the N data points from an external memory into an internal memory; computer readable code means for performing a FFT computation upon each one of the respective plurality of sets of data points of the N data points in the internal memory; and computer readable code means for providing instructions for performing an export of the respective plurality of sets of data points of the N data points from the internal memory into the external memory to update the respective plurality of sets of data points of the N data points in the external memory, wherein the stage groupings of at least one stage comprise a stage grouping of D stage and Q stage groupings of S stages wherein D, Q and S are integers and wherein said k substantially satisfies $k=QS+D$ and $k = \log_2(N)$, comprising further computer readable code means for:

grouping, within a stage grouping, I, of the Q stage groupings wherein I is an integer satisfying $0 \leq I \leq Q-1$, the N data points into 2^{IS} blocks of data of $N/2^{IS}$ respective data points;

grouping, within each one of the 2^{IS} blocks of data, the $N/2^{IS}$ respective data points into 2^S sub-blocks of data of $N/2^{IS+S}$ respective data points;

grouping, within each one of the 2^S sub-blocks of data, the $N/2^{IS+S}$ respective data points into M_1 sub-sub-blocks of data of $N/(2^{IS+S} M_1)$ respective data points wherein M_1 is an integer;

taking, within each one of the 2^{IS} blocks of data, a respective sub-sub-block of data of the M_1 sub-sub-blocks of data from each one of the 2^S sub-blocks of data to form a set of 2^S sub-sub-blocks of data of $N/(2^{IS} M_1)$ data points a total of M_1 times to produce M_1 sets of 2^S sub-sub-blocks of data of $N/(2^{IS} M_1)$ data points; and

taking, within each one of the M_1 sets of 2^S sub-sub-blocks of data, a respective data point from each one of the 2^S sub-blocks of data to form a set of 2^S data points a total of $N/(2^{IS+S} M_1)$ times to produce $N/(2^{IS+S} M_1)$ sets of 2^S data points.

42. (original) An article of manufacture according to claim 41 wherein, for the stage grouping, I, of the Q stage groupings of the plurality of stage groupings, the computer readable code FFT means is further adapted to perform M_1 of the plurality operations for each one of the 2^{IS} blocks of data within the stage grouping, I, and for each one of the M_1 of the plurality operations the computer readable code FFT means further comprising:

computer readable code means for providing instructions for performing an import of respective $N/(2^{IS+S}M_1)$ sets of 2^S data points from the external memory into the internal memory;

computer readable code means for performing an S-stage FFT computation of the k-stage FFT computation upon each set of 2^S data points of the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points in the internal memory; and

computer readable code means for providing instructions for performing an export of the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points from the internal memory into the external memory to update the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points in the external memory.

Feb 16, 2005

Patent Agent
Reg. No. 44,185

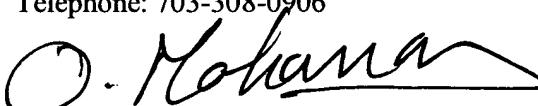
5 TROPIC NETWORKS INC.,
Intellectual Property Department
135 Michael Cowpland Drive
Kanata, Ontario, Canada.
K2M 2E9

10 Telephone: (613) 270-6026
FAX: (613) 270-9663
E-mail: Victoria.Donnelly@tropicnetworks.com

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25 Telephone: 703-308-0906


30 Omayma E. Moharram, Ph.D., P.Eng.
Patent Engineer,
TROPIC NETWORKS INC.,
Intellectual Property Department
135 Michael Cowpland Drive
Kanata, Ontario, Canada.
K2M 2E9

35 Telephone: (613) 270-6942
FAX: (613) 270-9663
E-mail: Omayma.Moharram@tropicnetworks.com

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